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10/719,469

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Vinod K. Balakrishnan

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EXAMINER

CHEA, PHILIP J

ART UNIT

PAPER NUMBER

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

# Office Action Summary

**Application No.**

10/719,469

**Applicant(s)**

BALAKRISHNAN, VINOD K.

**Examiner**

PHILIP J. CHEA

**Art Unit**

2153

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 27 December 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-28 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-28 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-946)
- 3) ☐ Information Disclosure Statement(s) (PTO/SG/US)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

### DETAILED ACTION

This Office Action is in response to an Amendment filed December 27, 2007. Claims 1-28 are currently pending. Any rejection not set forth below has been overcome by the current Amendment.

#### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claim 1,6-10,14,18,21,26,28 are rejected under 35 U.S.C. 102(e) as being anticipated by Cranor et al. (US 7,165,100), herein referred to as Cranor.

As per claim 1, Cranor discloses a method comprising:

processing network traffic using a first program, the first program containing a first interface instance having a first behavior (see column 3, lines 7-14, where the first program is considered one of the FTA processing blocks being performed by the processor on the NIC);

detecting a first condition (see column 3, lines 39-45, where detecting a first condition is considered detecting packets);

generating a second program, the second program containing a second interface instance having a second behavior (see column 3, lines 34-39, where new FTA blocks can be installed), the generation of the second program including selecting the second interface instance from a plurality of interface instances for inclusion in the second program and loading the second program for use in processing network traffic (see column 3, lines 39-45, where each FTA block may process packet data and column 3, lines 14-21, describing how the FTA blocks are program instructions that are loaded into the memory of the NIC and executed, and further evidence supporting the loading of new FTA blocks can be found in

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column 2, lines 1-5 and column 4, lines 1-4, describing how the next FTA block commences processing (i.e. it gets loaded to the processor for execution); and

processing network traffic using the second program (see column 3, lines 39-45).

As per claim 6, Cranor further discloses replacing the first program with the second program in at least one microengine, wherein the processing of the network traffic using the first and second programs is performed by said at least one microengine (see column 3, lines 16-19 and column 4, lines 16-20).

As per claim 7, Cranor further discloses that the first condition comprises a change in network traffic (see column 3, lines 39-45)

As per claim 8, Cranor further discloses detecting a second condition (i.e. the need for more FTA blocks);

generating a third program, the third program containing a third interface instance having a third behavior, the generation of the third program including selecting the third interface instance from a plurality of interface instances for inclusion in the third program (see column 3, lines 53-61); and processing network traffic using the third program (see column 3, lines 53-61).

As per claim 9, Cranor further discloses that the third program includes the second interface instance, the second interface instance corresponding to a different interface from the third interface instance (see column 3, lines 53-61, where each FTA performs different arbitrary functions).

As per claim 10, Cranor further discloses replacing a subroutine call in a copy of a master program with the second interface (see column 4, lines 16-20).

As per claim 14, Cranor further discloses that the first and second program are written in an instruction set of a microengine that performs the processing of network traffic using the first and second programs (see column 3, lines 14-19).

As per claims 18,26 Cranor discloses a system comprising:

a switch fabric (see Fig 1); and

one or more line cards comprising:

one or more physical layer components (see Fig. 1, [110]); and

on or more network processors, at least one of said network processors comprising:

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a processing core (see column 3, lines 7-9);

one or more microengines (see column 3, lines 9-14); and

a memory unit, the memory unit including code that, when executed by the processing core, is operable to cause the network processor to perform actions comprising:

detecting a first condition (see column 3, lines 39-45, where detecting a first condition is considered detecting packets);

identifying a first instance of a first interface suitable for handling the first condition (see column 3, lines 34-39, where new FTA blocks can be installed);

selecting the first instance of the first interface from a plurality of instances of the first interface (see column 3, lines 34-39);

generating a code image that includes the first instance of the first interface; and

loading the code image into one or more of the microengines for execution (see column 3, lines 39-45 and column 4, lines 1-4, describing how the next FTA block commences processing (i.e. it gets loaded to the processor for execution)).

As per claims 21,28, Cranor further discloses an instance resolver including code for detecting a first condition and identifying a first instance of a first interface suitable for handling the first condition (see column 3, lines 39-45, where detecting a first condition is considered detecting packets and the FTA notified to process the packets).

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 2,22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cranor as applied to claim 1 above and 18 below, and further in view of Knudsen ("LEGO Mindstorms Robots").

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As per claims 2,22 although the system disclosed by Cranor shows substantial features of the claimed invention (discussed above), it fails to disclose that the second interface instance is inlined into the second program, such that it is reachable without executing a jump or branch instruction.

Nonetheless, these features are well known in the art and would have been an obvious modification of the system disclosed by Cranor, as evidenced by Knudsen.

In an analogous art, Knudsen discloses a programming method that allows subroutines to be called inline. The compiler places the code inline wherever it is called (i.e. no jump or branch instruction) (see page 20, *Inlines*).

Given the teaching of Knudsen, a person having ordinary skill in the art would have readily recognized the desirability and advantages of modifying Cranor by employing inline subroutine, such as disclosed by Knudsen, in order to create a more robust program and easily read the source code.

5. Claims 3-5,16,19-20,24-25,27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cranor as applied to claim 1 above and claim 15 below, and further in view of Liberty ("Sams Teach Yourself C++ in 10 Minutes").

As per claims 3,16,19, although the system disclosed by Cranor shows substantial features of the claimed invention (discussed above), it fails to disclose interpreting a switch statement in a master program to locate the second interface instance; and

removing one or more interface instances other than the second interface instance from the master program.

Nonetheless, these features are well known in the art and would have been an obvious modification of the system disclosed by Cranor, as evidenced by Liberty.

In an analogous art, Liberty discloses that switch statements are old and well known (see page 77). At the time of the invention, a person having ordinary skill in the art would have found it obvious to use a switch statement to locate a second interface instance because *switch* statements are more efficient than *if* statements (i.e. execution jumps to a matching statement as opposed to running through the entire *if* statements).

In considering removing one or more interface instances other than the second interface instance from the master program, Cranor does show that a number of commands may be sent to a run-time system such as, removing FTA blocks, installing new FTA blocks, passing parameters to existing FTA blocks, etc. At the time of the invention, a person having ordinary skill in the art would have found it obvious to remove one or more other interface implementations from a first code image to form a second code image that includes the selected interface implementation, in order to save memory by removing code that is unused and needlessly taking up memory.

As per claim 4, Cranor further discloses that the one or more interface instances other than the second interface instance includes the first interface instance (see column 4, lines 1-4).

As per claim 5, Cranor further discloses that the generation of the second program is performed by a linker (see column 3, lines 21-24, where compiling inherently includes linking).

As per claims 20,24,25,27 Cranor further discloses it would be obvious that a linker interpret a switch statement and to remove unselected instances of an interface from the switch statement (see discussions above regarding switch statements and removing unused code in order to save memory).

6. Claims 11-13,15,17,23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cranor et al. (US 7,165,100), herein referred to as Cranor.

As per claims 15,23, Cranor discloses a method for performing dynamic resource adaptation, the method comprising:

identifying a selected interface implementation (see column 3, lines 34-39);

loading the second code image (see column 3, lines 14-21, describing how the FTA blocks are program instructions that are loaded into the memory of the NIC and executed, and further evidence supporting the loading of new FTA blocks can be found in column 2, lines 1-5 and column 4, lines 1-4, describing how the next FTA block commences processing (i.e. it gets loaded to the processor for execution);

using a second code image to perform one or more network processing tasks (see column 3, lines 34-39, where new FTA blocks can be installed).

Although the system disclosed by Cranor shows substantial features of the claimed invention (discussed above), it fails to disclose removing one or more other interface implementations from a first code image to form a second code image that includes the selected interface implementation.

However, Cranor does show that a number of commands may be sent to a run-time system such as, removing FTA blocks, installing new FTA blocks, passing parameters to existing FTA blocks, etc. At the time of the invention, a person having ordinary skill in the art would have found it obvious to remove one or more other interface implementations from a first code image to form a second code image that includes the selected interface implementation, in order to save memory by removing code that is unused and needlessly taking up memory.

As per claim 11, Cranor further discloses that it would be obvious that generating the second program comprises removing code from a third program (see discussion above regarding removing FTA blocks in order to save memory).

As per claim 12, Cranor does not expressly disclose that the second program is smaller than the third program. However, Cranor does show different sized programs (see Fig. 8A). At the time of the invention, a person having ordinary skill in the art would have found it obvious to have different sized programs in order to customize the programs for the specific tasks.

As per claim 13, Cranor does not expressly disclose that the first program and the second program comprise different versions of the same programs. However, Cranor does show program code that could easily be modified to create different versions (see Fig.8A). At the time of the invention, a person having ordinary skill in the art would have found it obvious to create different versions in order to make improvements over the previous versions or have different versions that are compatible with different hardware.

As per claim 17, Cranor further discloses a memory unit associated with a network processor, and in which the processor comprises a core processor of said network processor (see column 3, lines 7-9).



***Response to Arguments***

7. Applicant's arguments filed December 27, 2007 have been fully considered but they are not persuasive.

A) Applicant contends that Cranor does not disclose loading the second program for use in processing network traffic.

In considering A), the Examiner respectfully disagrees. Cranor shows that a second FTA block (i.e. program) is loaded for execution by the processor (see column 3, line 66 - column 4, line 4). The FTA is considered "loaded" because the FTAs are executed by the same or a different on-board processor (see column 3, lines 16-21). So when one FTA finishes its packet processing, the next is loaded into the processor for execution. Furthermore, it is implied that additional FTA blocks can be created and loaded into memory for later execution while packet processing has already started because Cranor discloses that the FTAs can be loaded and dynamically linked on-the-fly (see column 2, lines 8-10) and shows dynamic installation of new FTA blocks (see column 3, lines 34-39) and after packet processing by FTA blocks, the system can create new FTA for installation (see Fig. 2, *a flowchart showing packet processing by initial FTAs [201-203] and then receive commands to create new FTA instances* and column 4, lines 1-20, *describing how FTA blocks can be processing network traffic and then the system can respond to commands such as installing new FTA blocks*).

***Conclusion***

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action

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is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to PHILIP J. CHEA whose telephone number is (571)272-3951. The examiner can normally be reached on M-F 6:30-4:00 (1st Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Glenn Burgess can be reached on 571-272-3949. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Glenton Burgess/  
Supervisory Patent Examiner, Art Unit 2153

Philip J Chea  
Examiner  
Art Unit 2153

PJC 3/5/08